a first processor for providing successive sets of input data;

a second processor for receiving successive sets of output data;

a memory system including a plurality of memory circuits where all of the plurality of memory circuits are accessible by the first processor and the second processor;

a master controller for setting up the plurality of memory circuits of said memory system using control commands associated with a set of input data and a set of output data; and

a control unit for, on the basis of the control commands, ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of independent memory circuits.

4. (Amended) A memory system comprising:

a plurality of memory circuits for receiving successive sets of input data and for providing successive sets of output data, all of the plurality of memory circuits being accessible by at least two processors;

a control unit being programmable by means of control commands associated with a set of input data and a set of output data and, on the basis of these control commands, for ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of memory circuits.

5. (Amended) A method of processing data in a data processing arrangement including a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system including a plurality of memory circuits that are all accessible by both the first and processor and the second